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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,049	12/22/2004	Marcin Stabrowski	LHUD-01001-NUS	6760

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
05/18/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/519,049	STABROWSKI, MARCIN	
	Examiner	Art Unit	
	Bryce P. Bonzo	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/22/05,6/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-8 are rejected under 35 USC §103.

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (United States Patent No. 4,627,060).

As per the claims, Huang discloses:

1. A circuit for detection of *external* microprocessor watchdog device execution comprising a microprocessor with the internal watchdog device (Figure 3, item 10), an input/output line transmitting information about microprocessor reset (item 80), and a device for resetting the microprocessor system (item 80), wherein to the input/output line (11) transmitting information about the microprocessor (6) reset (Item 80), a clock input CK is connected, which triggers the flip-flop (12), whose data input D and an inverted reset input /R are connected to an output of the device (19) for resetting the microprocessor, and an inverted flip-flop (12) output /Q is connected to an input of the

device (19) for resetting the microprocessor (column 2, line 59 through column 3, lines 10).

Huang does not explicitly disclose the internal integration of a watchdog timer into a microprocessor. Official Notice is given that it is well known to integrate ancillary support devices on to the main silicon of a microprocessor. Since the mid-1980s, rapid advances in the scale of lithography and circuit design have led to numerous devices being incorporated in microprocessors, including: JTAG, level 1 caches, level 2 caches, among others. This is done as the bonding and connection to circuitry from one package to another is fraught with hazards. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the external watchdog design of Huang into a know microprocessor, thus following the industry trend of integration.

As per claim 2, Huang discloses:

The circuit according to claim 1, further comprising an external resistor (10) connecting the input/output line (11) transmitting information about microprocessor (6) reset to a power supply voltage (V.sub.cc) (Fig 1b: +5v, 33kΩ at the termination of line 80).

As per claim 3, Huang discloses:

The circuit according to claim 1, wherein reset of the microprocessor system resulting from the reset of the microprocessor (6) is performed when the inverted reset input /R

and the flip-flop (12) data input D are in a high state and the clock input CK changes from a low to a high state (Figure 1c:30).

4. The circuit according to claim 1, wherein reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by a low state of the inverted reset input /R of the flip-flop (12) (Abstract).

As per claim 5, Huang discloses:

A method for reset of a microprocessor system with a circuit for detection of *external* microprocessor watchdog device execution comprising the following steps:

setting an input/output line (11) of a microprocessor to a high impedance state after disruption of microprocessor operation (Figure 1);

sending a system reset signal, generated by a flip-flop (12), to a device for resetting the microprocessor system (column 3, lines 59-column 4, line 40); and

setting the input/output line (11) to a low state after finishing the resetting of the microprocessor system (column 3, lines 59 through line 10).

Huang does not explicitly disclose the internal integration of a watchdog timer into a microprocessor. Official Notice is given that it is well known to integrate ancillary support devices on to the main silicon of a microprocessor. Since the mid-1980s, rapid advances in the scale of lithography and circuit design have led to numerous devices being incorporated in microprocessors, including: JTAG, level 1 caches, level 2 caches,

among others. This is done as the bonding and connection to circuitry from one package to another is fraught with hazards. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the external watchdog design of Huang into a know microprocessor, thus following the industry trend of integration.

6. The method according to claim 5, wherein the microprocessor system is reset, when the flip-flop (12) has an inverted reset input /R, a data input D and a clock input CK, and the inverted reset input /R and the data input D are in a high state and the clock input CK changes from a low to a high state (figure 1c: 30).

7. The method according to claim 5, wherein the reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by imposing a low state on the flip-flop (12) inverted reset input /R (Abstract).

Claim 8 is considered a rewritten form of claim 1 and 2, without the legacy verbiage from the original Polish document, and is rejected on the same grounds.

Examiner's Remarks

Every attempt was made to examine the claims despite the clear importation of European drafting claim style and generally narrative claim translation. Applicant is strongly encouraged to being these claims in to proper United States form.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bryce P. Bonzo
Primary Examiner
Art Unit 2113